

IN THE CLAIMS

1. (Currently Amended) Assembly process of at least one electronic component (1) including sensibly flat conductive areas (3) that are connected to conductive tracks (6') placed on the surface of a generally flat insulating support called a substrate (5) characterized by the following steps:

- placing the substrate (5) on a work surface, the face including conductive tracks (6') being oriented upwards,
- placing the electronic component- (1) into a cavity (7) of the substrate (5) situated in a zone including the conductive tracks-(6'), the conductive areas (3) of the component (1) coming into contact with the corresponding tracks (6') of the substrate-(5),
- applying a layer of insulating material (8) which extends at the same time on the component (1) and at least on a substrate zone surrounding said component-(1), in such a way that the electric connection between the conductive areas (3) and conductive tracks-(6') is ensured by the pressure of the insulating layer (8) on the component-(1).

2. (Currently Amended) Process according to claim 1 ~~characterized in that~~ wherein the electronic component (1) is made up of a chip (2) provided with contacts on one of its faces, said contacts being set off on a conductive film constituting the contact areas that extend the contacts of the chip-(2), the opposite face of the chip being coated by an insulating material (4).

3. (Currently Amended) Process according to claim 1 ~~characterized in that~~ wherein the layer of insulating material is made up of a first substrate (5) including a cavity (7) into which the component (1) is inserted by its coated face, the contact areas (3) of said component (1) connecting with corresponding conductive areas (6) of a second substrate (9) placed on the work surface.

4. (Currently Amended) Process according to claim 1 ~~characterized in that~~ wherein the electronic component (1) is made up of a chip (2) provided with contacts on one of its faces, said contacts being set off on a conductive film constituting the contact areas (3) that extend the contacts of the chip-(2).

5. (Currently Amended) Process according to claims 1 ~~and 4 characterized in that~~ wherein the electronic component is made up of a chip provided with contacts on one of its faces, said contacts being set off on a conductive film constituting the contact areas that extend the contacts of the chip, the layer of insulating material is made up of a first substrate (5) including a cavity (7) in which the chip (2) of the component (1) is inserted, the contact areas (3) of said component (1) being applied against the surface of the substrate (5) connecting with corresponding conductive areas (6) of a second substrate (9) placed on the work surface.

6. (Currently Amended) Process according to ~~claims 1 and 4~~ claim 5 characterized in that wherein the cavity (7) of the component (1) is obtained by heating the chip (2) of the component (1) then pushing said chip (2) into the substrate (5) material by means of adequate tooling, the contact areas (3) of said component (1) being applied against the surface of the substrate (5).

7. (Currently Amended) Process according to claim 1 ~~characterized in that~~ wherein the electronic component (1) is made up of a chip (2) provided with sensibly flat contacts on one of its faces.

8. (Currently Amended) Process according to claim 7 ~~characterized in that~~ wherein the layer of insulating material is made up of a first substrate (5) including a cavity (7) into which the chip (2) is inserted, the contacts of said chip showing on the surface level of the substrate are connected with corresponding conductive areas (6) of a second substrate (9) placed on the work surface.

9. (Currently Amended) Process according to claim 1 ~~characterized in that~~ wherein the cavity (7) of the component (1) is made up by milling or by stamping a window.

10. (Currently Amended) Process according to claim 8 ~~characterized in that~~ wherein the cavity (7) of the chip (2) is obtained by heating then pressing said chip (2) into the material of the substrate (5) by means of adequate tooling, the contact areas of said chip (2) showing on the surface level of the substrate.

11. (Currently Amended) Process according to claim 1 ~~characterized in that~~ wherein the electronic component (1) is made up of a module including a set of flat contacts on one of its faces and on the opposite face conductive areas linked to each contact of the set.

12. (Currently Amended) Process according to claims 1 ~~and 11 characterized in that~~ wherein the module is inserted into a cavity (7) provided with a window cut into a first substrate (5) with a thickness approximately equal to that of the module, the set of flat contacts shows on the surface level of said substrate (5) and the conductive areas of the opposite face lean against the conductive tracks (6) of a second substrate (9) assembled on the first substrate (5).

13. (Currently Amended) Process according to claim 12, ~~characterized in that~~ wherein at least one module or a supplementary chip (2) is mounted in one of the substrates ~~(5, 9)~~, said module including conductive areas (3) connected by pressure on the corresponding conductive tracks (6) of either of the substrates ~~(5, 9)~~.

14. (Currently Amended) Process according to claims 3 ~~and 13 characterized in that~~ wherein it includes a supplementary step of gluing and pressing the assembly formed by the superposition of the substrates ~~(5, 9)~~.